METHOD AND APPARATUS FOR TESTING CIRCUITRY EMBEDDED WITHIN A FIELD PROGRAMMABLE GATE ARRAY

ABSTRACT OF THE INVENTION

A circuit that includes a core device that is embedded within fixed interfacing logic circuitry that, in turn, is embedded in an FPGA fabric. The FPGA fabric may be configured into a test mode of operation to test either the embedded device or fixed logic devices formed within the fixed interfacing logic. While the FPGA is configured in a test mode, test circuitry and communication paths are made present within the fixed interfacing logic circuitry to facilitate the testing. Additionally, the test circuitry comprises isolation circuitry that is formed between various modules and circuits that are to be tested to isolate the device under test and to produce test signals thereto and therefrom during testing operations.